Coplanar Stripline Components for High-Frequency Applications

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***Abstract*— In this paper, coplanar stripline (CPS) discontinuities such as a narrow transverse slit, a symmetric step, a right-angle bend, and a T-junction are characterized and their performance is parameterized with respect to frequency and geometry. In addition, filter design using coplanar stripline discontinuities has been investigated. Lumped equivalent circuits are presented for some of the discontinuities. The element values are obtained from the measured discontinuity scattering parameters. The experimental results are compared with theoretical data obtained using the finite-difference time-domain (FDTD) technique for validation and show very good agreement.**

***Index Terms*—Band-stop filters, coplanar stripline, discontinuities, FDTD technique, scattering parameters, TRL calibration, uniplanar circuits.**

I. Introduction

As with a coplanar waveguide (CPW), the coplanar stripline (CPS) [1] was introduced in the mid-1970's as a transmission medium with the capability to provide uniplanar designs. Due to its balanced configuration, it has found wide applicability in feed networks for printed antennas [2], [3]. As the application moves to higher frequencies and the size of the substrate becomes critical in triggering parasitic modes and uncontrolled radiation, lines which show less dependence on wafer thickness become better candidates. Among these lines, the CPW has attracted much more attention despite the limitations imposed by its large ground planes and the excitation of parallel-plate parasitic modes. The use of many vias to suppress these parasitic modes introduces many difficulties in the design and fabrication resulting in poor performance and high cost. In view of the above disadvantages, coplanar lines with finite-size grounds such as the CPS require more attention. The CPS has the capability to provide excellent propagation [4]. When appropriately designed, it has small discontinuity parasitics, makes efficient use of the wafer area, and can sustain back metallization without exciting parasitic modes within the range of the operating frequency. Lastly, heat sinking and packaging in high-power applications (CPS power amplifiers) is simplified.

Some CPS discontinuities such as an open circuit, short circuit, series gap, spur-slot, and spur-strip have been extensively studied and characterized in the past [5]. This paper presents an extensive characterization of some additional CPS discontinuities, such as a narrow transverse slit, symmetric step, right-angle bend, and a T-junction. The equivalent-circuit model-element values for these discontinuities are determined from the scattering parameters (S-parameters) which are de-embedded from the measured S-parameters using a thru-reflect-line (TRL) algorithm. The circuits are fabricated on a 762-μm-thick RT-Duroid 6010 substrate ($\epsilon_r = 10.2$) having 0.5-oz copper cladding. The experimental results are compared to data obtained using the finite-difference time-domain (FDTD) method for validation. The results of the CPS discontinuities studied above indicate potential applications in the emerging wireless communications industry in general, and in the design of low-cost uniplanar microwave circuits such as filters, mixers, and antennas in particular. This has been demonstrated by fabricating bandstop filters using CPS discontinuities. The performances of a few of these filters are presented. Here too, the measured filter response is compared with the results obtained by modeling the filter using the FDTD technique.

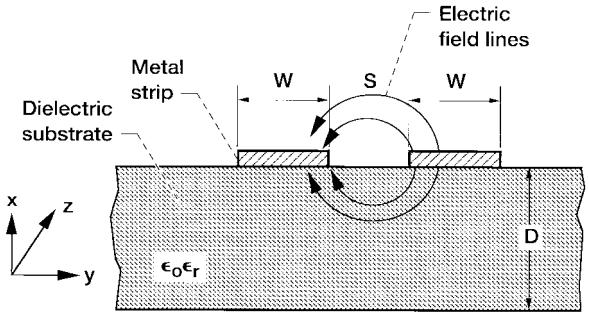

Fig. 1. Cross section of CPS.

II. Theoretical and Experimental Characterization

In a CPS [1], the electric-field lines from the strip conductors of width W extend across the slot of width S. The CPS is supported on a thin dielectric substrate of relative permittivity ϵ_r and thickness D, as shown in Fig. 1. This paper presents the study of several CPS discontinuities (see Figs. 2, 7, 9, 11, and 13) which find use in monolithic microwave integrated circuits (MMIC's). The study is performed both theoretically as well as experimentally and the two sets of results are compared for validation purposes.

A. Experimental Characterization

The measurements have been performed with an automatic network analyzer (HP8510C) using a TRL calibration technique. This technique utilizes on-wafer standards along with a pair of ground-signal RF probes [5]. The standards consist

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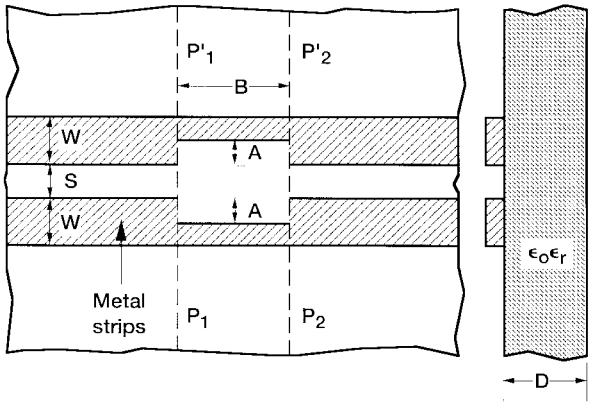

Fig. 2. Symmetric transverse slit and a step in the CPS strip conductors.

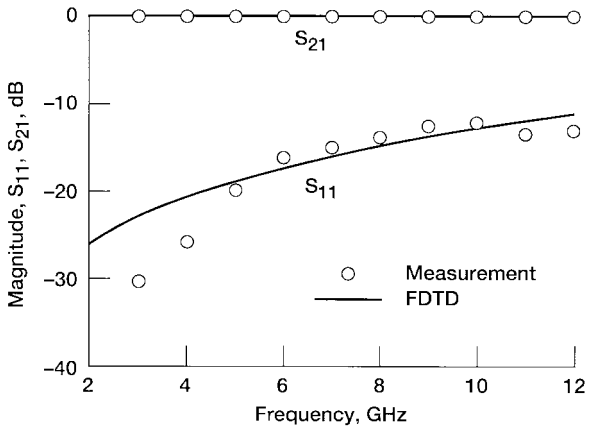

Fig. 3. Experimental and FDTD modeled magnitude of S_{11} and S_{21} for CPS slit. $A = 531.9$ μm, $B = 180.3$ μm.

of a CPS thru, a CPS short circuit, and a CPS delay line. The network analyzer is calibrated using National Institute of Standards and Technology (NIST) de-embedding software.[1] The reference impedance is set by the characteristic impedance Z_o of the delay line.

B. Theoretical Modeling

As mentioned above, the modeling was performed using the FDTD method, [6]–[9], which is based on expressing Maxwell's curl equations in discretized space and time domains. In order to characterize any planar discontinuity, propagation of a specific time-dependent function is simulated using the FDTD technique. In characterizing the discontinuities mentioned above, a Gaussian pulse was used. The space steps Δx, Δy, and Δz are carefully chosen such that integral numbers of them can approximate the dimensions of the structure. The Courant stability criterion is used to select the time step to ensure numerical stability. It is important to note at this point that the circuit dimensions indicated in the following figures are the actual dimensions after fabrication. However, while performing the FDTD analysis, the exact fabricated dimensions could not be incorporated due to limitations in the uniform discretization adopted in the modeling.

[1]NIST de-embedding software, program DEEMBED, Rev. 4.04, 1994.

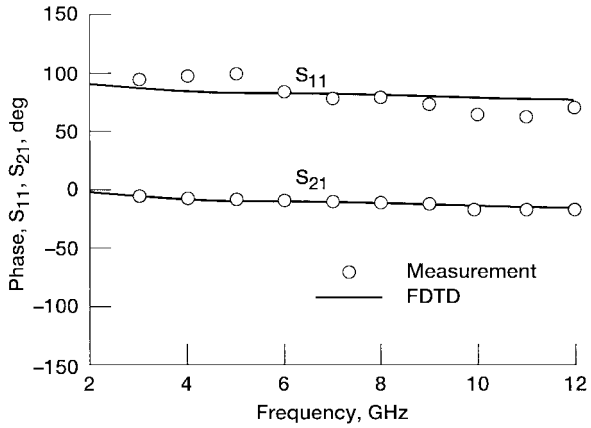

Fig. 4. Experimental and FDTD modeled phase of S_{11} and S_{21} for CPS slit. $A = 531.9$ μm, $B = 180.3$ μm.

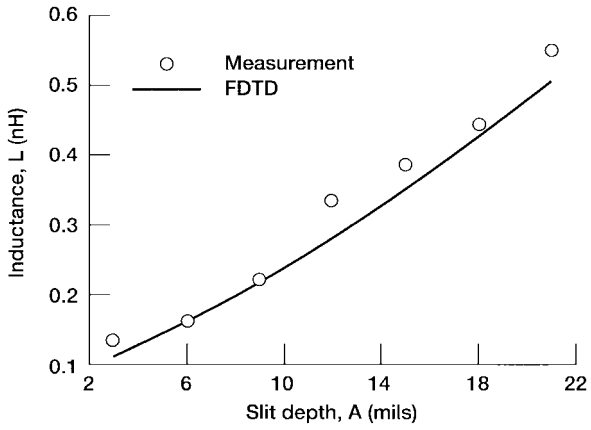

Fig. 5. Inductance determined from the de-embedded S-parameters and FDTD model as a function of slit depth at 9 GHz.

III. Results and Discussion

In the following section, results for a narrow transverse slit on a CPS line, a symmetric CPS step (Fig. 2), a CPS right-angle bend (Fig. 7), a CPS T-junction (Fig. 9), a CPS spur-slot bandstop filter (Fig. 11), and a CPS spur-strip bandstop filter (Fig. 13) are presented. For all the discontinuities considered here the slot width is 101.6 μm and the strip width is 762 μm, unless otherwise specified.

A. Narrow Transverse Slit and a Symmetric Step in the CPS Strip Conductor

A symmetric narrow slit of width B and depth A in the CPS strip conductor is shown in Fig. 2. The slit is modeled as a lumped inductor L located between the planes P_1–P_1' and P_2–P_2' in series with the line. The inductance is determined from the discontinuity S-parameters of the circuit, which are de-embedded from the measured S-parameters of the circuit. Figs. 3 and 4 show plots of the de-embedded and FDTD modeled scattering parameters as a function of frequency for a slit of depth $A = 531.9$ μm and width $B = 180.3$ μm. Fig. 5 shows the series inductance as a function of the slit depth A when the width B is held constant at 180.3 μm. As expected, the inductance increases with the slit depth.

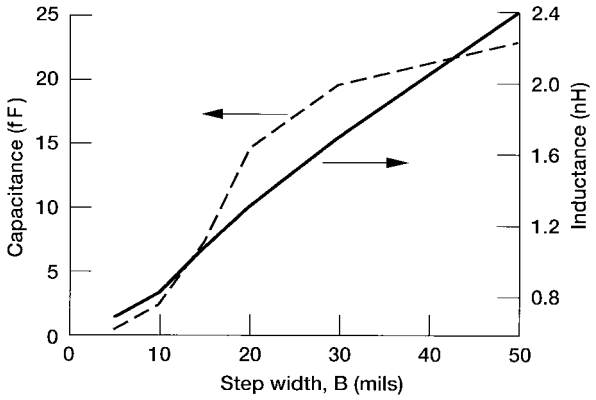

Fig. 6. Lumped fringing capacitance and series inductance determined from the de-embedded measured S-parameters as a function of step width at 6 GHz.

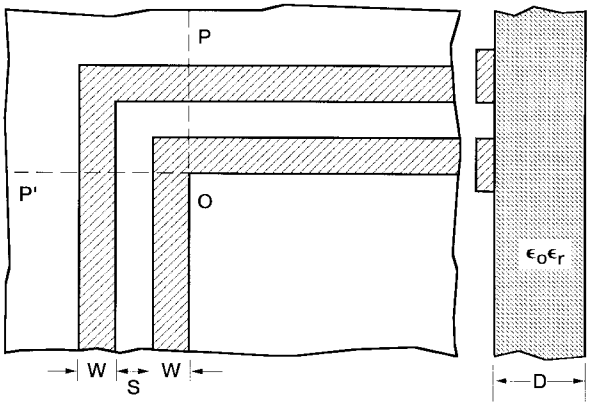

Fig. 7. CPS right-angle bend.

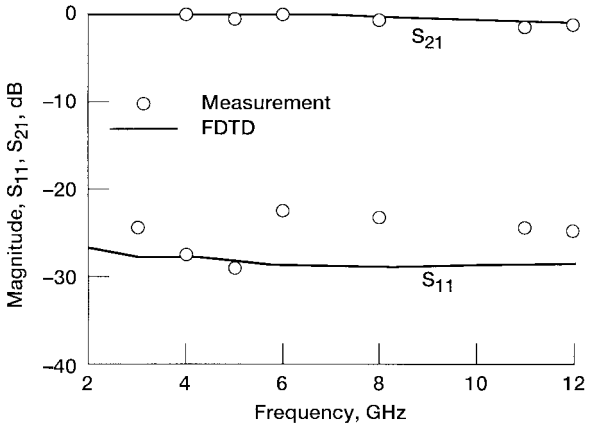

Fig. 8. Experimental and FDTD modeled magnitude of S_{11} and S_{21} as a function of frequency for CPS bend. $S = 101.6$ μm.

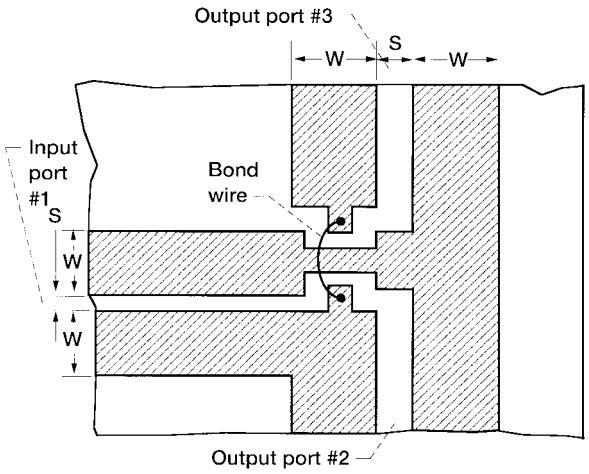

Fig. 9. CPS T-junction.

It would be noteworthy at this point that for small values of the slit width, the discontinuity can be modeled purely as an inductance to a very close degree of accuracy. The slight difference between the measured and FDTD results in Figs. 3–5 can be attributed to the difference in dimensions between the fabricated structure and FDTD model.

However, if the slit depth is kept constant and the slit width B is varied, the discontinuity can no longer be modeled purely as an inductive element. For larger slit widths, the discontinuity which is now a CPS step, needs to be modeled as a π-equivalent *LC* circuit where the capacitance, C, is the fringing capacitance and the inductance L is the series inductance. Fig. 6 plots the lumped fringing capacitance C and the series inductance L for a CPS step as a function of the step width at a frequency of 6 GHz for a fixed depth A of 533.4 μm. As expected, the capacitance is initially small, increases with step width, and eventually saturates. The measured scattering parameters for a typical slit step has been validated using the FDTD technique and are presented in Figs. 3 and 4. Hence, the FDTD modeling was not repeated for the remaining step widths. Consequently, Fig. 6 excludes the FDTD modeled equivalent lumped-circuit element values.

B. CPS Right-Angle Bend

A CPS right-angle bend is shown in Fig. 7. Several CPS bends have been fabricated with slot width ranging from 110 μm (4.33 mil) to 230 μm (9.06 mil) and the strip width fixed at 762 μm (30 mil). In all cases, it was seen that de-embedded measured S-parameters as well as the FDTD method show the reflection to be of the order of -20 dB or lower. Fig. 8 presents the results for a typical right-angle bend. Hence, it was concluded that compensation of the bend to improve VSWR is not required. This fact is used in the design of a CPS T-junction which follows next where the CPS line is bent at a few places without resulting in any noticeable parasitics due to the bend. Although Fig. 8 indicates low reflection losses for measured as well as modeled cases, it can be seen that the return loss in the case of FDTD modeling is lower. It is also seen that the measured magnitude of S_{21} is slightly lower than the S_{21} obtained by FDTD modeling. These differences can be attributed to the calibration accuracy of the measured results and to the fact that the FDTD scheme adopted here does not take losses into account.

C. CPS T-Junction

A CPS in-phase T-junction is shown in Fig. 9. The measured and FDTD modeled magnitude of S_{11}, S_{21}, and S_{31} as a function of frequency is shown in Fig. 10. As seen from the figure, power is almost equally divided between the output

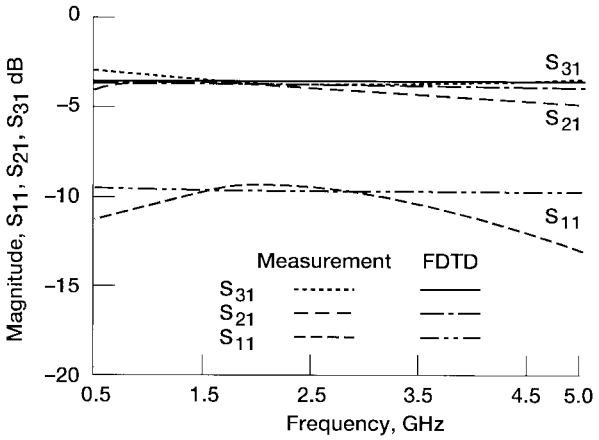

Fig. 10. Experimental and FDTD modeled magnitude of S_{11}, S_{21}, and S_{31} for a T-junction.

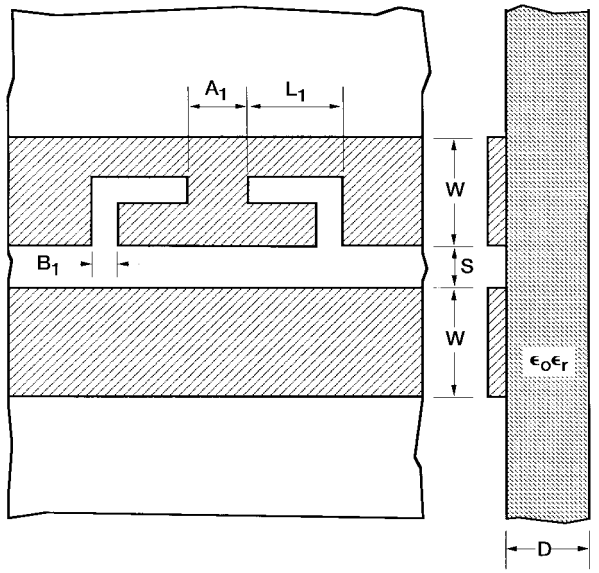

Fig. 11. CPS spur-slot bandstop filter.

ports 2 and 3. It was also observed that the phase of S_{31} and S_{21} was equal as expected. From Fig. 10 it is seen that there is a very good agreement between the measured and FDTD modeled power coupled to the two output ports.

D. CPS Bandstop Filters

The configuration of a CPS spur-slot bandstop filter is shown in Fig. 11. The spur-slot is convenient to use when W is large and S is small. It can be modeled as a short-circuit stub of length $L = \lambda_{g(\mathrm{cps})}/4$ in series with the main line. At resonance, the stub prevents the flow of RF power to the load. The measured and modeled S_{11} and S_{21} for the geometry is shown in Fig. 12. On the other hand, the spur-strip is convenient to use when W is small and S is large and can be modeled as two open circuit stubs each of length $L_1 = \lambda_{g(\mathrm{cps})}/4$ in parallel with the main line. Fig. 13(a) shows the configuration of a CPS spur-strip bandstop filter with a taper on either end. This was the configuration for which measurement was performed. Fig. 13(b) shows the configuration that was used to perform the FDTD modeling. Tapers were included in

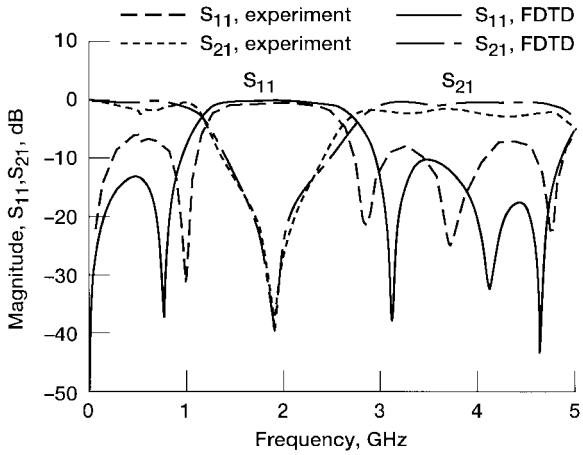

Fig. 12. Experimental and FDTD modeled magnitude of S_{11} and S_{21} for a spur-slot bandstop filter. $A_1 = 762\ \mu$m, $B_1 = 254\ \mu$m, and $L_1 = 16.256$ mm.

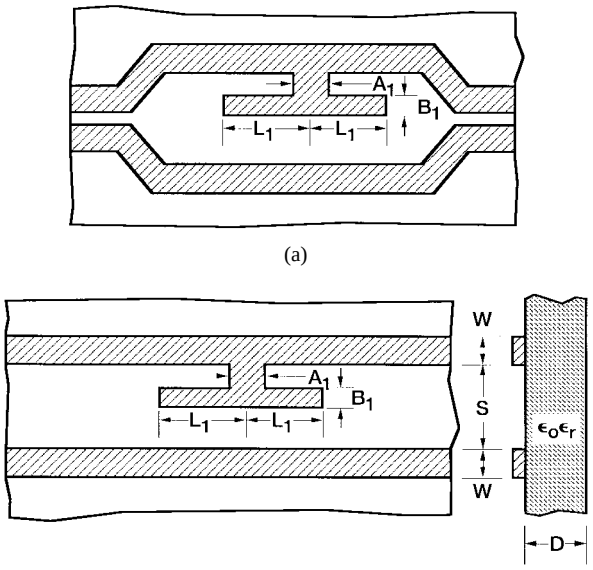

Fig. 13. (a) CPS spur-strip bandstop filter used in the measurement. (b) CPS spur-strip bandstop filter used in modeling.

the measurement to accommodate a ground-signal RF probe of 254-μm (10-mil) pitch. However, while simulating the results using the FDTD method, the tapers were eliminated due to memory constraints. Fig. 14 shows the magnitude of measured and modeled S-parameters for the spur-strip filter. From Figs. 12 and 14, we see that there is a good agreement in the measured and modeled resonance frequency for both the filters. However, Fig. 14 shows a slight difference between the measured and modeled S_{21} for the spur-strip filter. This can be attributed to the tapers being excluded in the FDTD modeling. It is interesting to note that the spur-strip filter has a narrower bandwidth compared to the spur-slot filter indicating that the strip filter has a higher quality factor (Q) compared to the slot filter. As a point of interest, it is worthwhile mentioning that a spur-slot with four slots (with the two extra slots being a mirror image of the previous two) has the same resonance as the spur-slot structure in Fig. 11, but a broader bandwidth (lower Q).

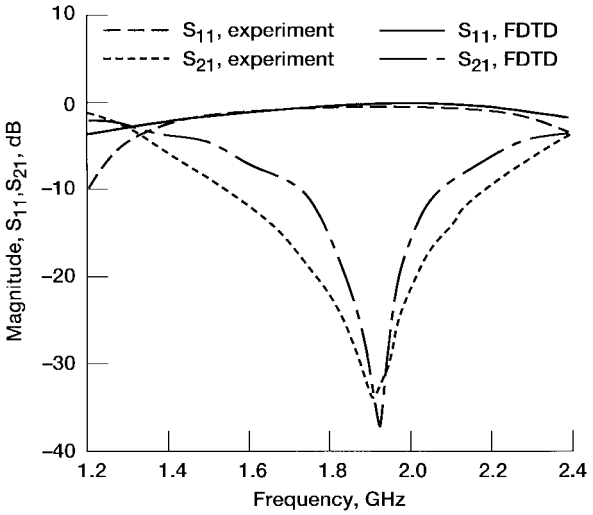

Fig. 14. Experimental and FDTD modeled magnitude of S_{11} and S_{21} for a spur-strip bandstop filter. $A_1 = 254$ μm, $B_1 = 254$ μm, $L_1 = 16.129$ mm, and $S = 762$ μm.

IV. Conclusion

The CPS as a transmission medium holds a great deal of potential because of several advantages, such as excellent propagation, small discontinuity parasitics, and efficient use of the wafer area. In view of these advantages, modeling of some CPS discontinuities which have several technical and commercial applications, was performed as a function of frequency and geometry. Good agreement was found between the experimental and theoretical results.

Acknowledgment

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References

[1] J. B. Knorr and K. D. Kuchler, "Analysis of coupled slots and coplanar strips on dielectric substrate," *IEEE Trans. Microwave Theory Tech.*, vol. MTT-23, pp. 541–548, July 1975.

[2] R. N. Simons, G. E. Ponchak, R. Q. Lee, and N. S. Fernandez, "Coplanar waveguide fed phased array antenna," in *IEEE Antennas Propagat. Int. Symp. Dig.*, vol. 4, Dallas, TX, May 1990, pp. 1778–1781.

[3] R. N. Simons, N. I. Dib, R. Q. Lee, and L. P. B. Katehi, "Integrated uniplanar transition for linearly tapered slot antenna," *IEEE Trans. Antennas Propagat.*, vol. 43, pp. 998–1002, Sept. 1995.

[4] M. Y. Frankel, J. F. Whitaker, and G. A. Mourou, "Optoelectronic transient characterization of ultrafast devices," *IEEE J. Quantum Electron.*, vol. 28, pp. 2313–2324, Oct. 1992.

[5] R. N. Simons, N. I. Dib, and L. P. B. Katehi, "Modeling of coplanar stripline discontinuities," *IEEE Trans. Microwave Theory Tech.*, vol. 44, pp. 711–716, May 1996.

[6] X. Zhang and K. K. Mei, "Time-domain finite difference approach to the calculation of the frequency-dependent characteristics of microstrip discontinuities," *IEEE Trans. Microwave Theory Tech.*, vol. 36, pp. 1775–1787, Dec. 1988.

[7] K. K. Mei and J. Fang, "Superabsorption—A method to improve absorbing boundary conditions," *IEEE Trans. Antennas Propagat.*, vol. 40, pp. 1001–1010, Sept. 1992.

[8] T. Shibata and H. Kimura, "Computer-aided engineering for microwave and millimeter-wave circuits using the FDTD technique of field simulations," *Int. J. Microwave Millimeter-Wave Comput.-Aided Eng.*, vol. 3, no. 3, pp. 238–250, May 1993.

[9] N. I. Dib, R. N. Simons, and L. P. B. Katehi, "New uniplanar transitions for circuit and antenna applications," *IEEE Trans. Microwave Theory Tech.*, vol. 43, pp. 2868–2873, Dec. 1995.

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